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For: METHOD OF MANUFACTURING	) Art Unit: 2813
A SEMICONDUCTOR FILM WITH LITTLE WARP	)

Honorable Commissioner of Patents and Trademarks  
Alexandria, VA 22313-1450

VERIFICATION OF TRANSLATION

Sir:

I, Yukiko Kokubu, 307-1, Hase, Atsugi-shi, Kanagawa-ken 243-0036 Japan, a translator, herewith declare:

that I am well acquainted with both the Japanese and English Languages;

that I am the translator of the attached translation of the Japanese Patent Application No. 2001-055436 filed on February 28, 2001; and

that to the best of my knowledge and belief the followings is a true and correct translation of the Japanese Patent Application No. 2001-055436 filed on February 28, 2001.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Date: this 13<sup>th</sup> day of June 2005

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[Attachment] Abstract

[Proof] required

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[Title of the Invention]

## METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

[Scope of Claim]

5

[Claim 1]

A method of manufacturing a semiconductor device, characterized in the steps of:  
adding a metal element to an amorphous semiconductor film;  
performing a first heat treatment on said amorphous semiconductor film added with  
said metal element to form a first crystalline semiconductor film by;  
10 recrystallizing said first crystalline semiconductor film by irradiating with a laser  
beam to form a second crystalline semiconductor film having a strain;  
performing a second heat treatment on said second crystalline semiconductor film at a  
higher temperature than said first heat treatment to lessen said strain.

15

[Claim 2]

A method of manufacturing a semiconductor device, characterized by the steps of:  
forming an amorphous semiconductor film on an insulating surface;  
adding a metal element to said amorphous semiconductor film;  
performing a first heat treatment on said amorphous semiconductor film added with  
20 said metal element to form a first crystalline semiconductor film by;  
recrystallizing said first crystalline semiconductor film by irradiating with a laser  
beam to form a second crystalline semiconductor film having a strain.  
performing a second heat treatment on said second crystalline semiconductor film at a  
higher temperature than said first heat treatment to lessen said strain;  
25 etching said second crystalline semiconductor film after said second heat treatment to  
form a second crystalline semiconductor film island.

30

[Claim 3]

A method of manufacturing a semiconductor device, characterized by the steps of:  
forming an amorphous semiconductor film on an insulating surface;  
adding a metal element to said amorphous semiconductor film;  
performing a first heat treatment on said amorphous semiconductor film added with  
said metal element to form a first crystalline semiconductor film by;  
35 recrystallizing said first crystalline semiconductor film by irradiating with a laser  
beam to form a second crystalline semiconductor film having a strain;  
etching said second crystalline semiconductor film to form a second crystalline  
semiconductor film island;  
performing a second heat treatment on said second crystalline semiconductor film  
island at a higher temperature than said first heat treatment to lessen said strain.

40

[Claim 4]

A method of manufacturing a semiconductor device according to any one of claims 1  
to 3, characterized in that:

said laser beam is the light emitted by excimer laser, YAG laser, YVO<sub>4</sub> laser, YAlO<sub>3</sub>

laser, or YLF laser.

[Claim 5]

5 A method of manufacturing a semiconductor device according to any one of claims 1 to 4, characterized in that:

said laser beam forms a linear shape or a rectangular shape on the irradiated surface or in the vicinity thereof.

[Claim 6]

10 A method of manufacturing a semiconductor device according to any one of claims 1 to 3, characterized in that:

said heating treatment is carried out by thermal annealing using a furnace annealing oven.

[Claim 7]

15 A method of manufacturing a semiconductor device according to any one of claims 1 to 3, characterized in that:

said heating treatment is performed by radiating a lamp light.

[Claim 8]

20 A method of manufacturing a semiconductor device according to any one of claims 1 to 3, and claims 6 and 7 characterized in that:

the heating time of said heat treatment one to 30 minutes.

[Claim 9]

25 A method of manufacturing a semiconductor device according to claim 7 characterized in that:

a temperature rising rate and a temperature lowering rate for said lamp light irradiation are within a range of 30 to 300°C /minute.

[Claim 10]

30 A method of manufacturing a semiconductor device according to claim 7 or 9 characterized in that:

35 said lamp light is radiated from at least one of an upper side and a lower side of a substrate.

[Claim 11]

A method of manufacturing a semiconductor device according to claim 7, 9, or 10 characterized in that:

5 said lamp light is radiated from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, and a high pressure mercury lamp.

[Claim 12]

A method of manufacturing a semiconductor device according to any one of claims 1 to 3, characterized in that:

10 said amorphous semiconductor film is formed through LPCVD method or a sputtering method.

[Claim 13]

15 A method of manufacturing a semiconductor device according to any one of claims 1 to 3, characterized in that:

said amorphous semiconductor film is formed through a plasma CVD method at 400°C or higher.

[Claim 14]

20 A method of manufacturing a semiconductor device according to any one of claims 1 to 3, characterized in that:

said metal element comprises one or a plurality of the elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au, Sn and Sb.

[Claim 15]

25 A method of manufacturing a semiconductor device according to any one of claims 1 to 14, characterized in that:

said semiconductor device is liquid crystal display device or a light emitting device.

[Claim 16]

30 A method of manufacturing a semiconductor device according to any one of claims 1 to 14, characterized in that:

said semiconductor device is one selected from the group consisting of a cellular phone, a video camera, a digital camera, a projector, a goggle type display, a personal computer, DVD player, or a mobile information terminal.

35

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention pertains]

5 The present invention relates to a method of manufacturing a semiconductor device, which includes a process of annealing a semiconductor film using a laser beam (hereinafter referred to as laser annealing). Semiconductor devices herein include electro-optical devices such as liquid crystal display devices and light emitting devices, and electronic equipment that contains the electro-optical devices as components.

[0002]

10 [Prior Art]

In recent years, a technique of performing either or both of heat treatment and laser annealing to crystallize a semiconductor film formed over an insulating substrate made of glass or the like, and to improve the crystallinity of the film, has been extensively studied. Silicon is often used for the semiconductor film. In this specification, laser crystallization refers to a method of crystallizing a semiconductor film by means of the laser beam to obtain a crystalline semiconductor film. Note that, in this specification, the crystalline semiconductor film refers to the semiconductor film in which crystallized areas exist.

[0003]

20 The crystalline semiconductor film formed through the crystallization described above possesses high mobility. For this reason, thin film transistors (TFT) are formed by means of this crystalline semiconductor film. And for example, this crystalline semiconductor film is quite often employed in monolithic type liquid crystal electro-optical devices in which TFTs for driving pixels and TFTs for driver circuits are formed on a single glass substrate.

[0004]

25 As described above, the crystalline semiconductor film has extremely better properties than an amorphous semiconductor film. For this reason, the above-mentioned study has been conducted. For crystallizing the amorphous semiconductor film by heating, for example, the heating temperature of 600°C or higher and the heating time of 10 hours or longer, preferably 20 hours or longer were required. Among the substrates that can withstand the crystallization conditions is a quartz substrate, for example. However, the quartz substrate is expensive, and it was extremely difficult to process the quartz substrate into a large-sized substrate in particular. Enlarging substrates is especially essential for increasing production efficiency. Recently, there is a remarkable trend toward larger-sized substrates so as to improve the production efficiency. Therefore, on production lines of a factory to be newly constructed, a substrate size

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of 600 × 720 mm is becoming the standard.

[0005]

Among glass substrates that have a comparatively high melting point is a 1737 glass substrate. Strain point of the glass substrate is 667°C, a temperature point or a temperature  
5 from which a change in shape of the 1737 glass substrate becomes manifest (annealing point) is 721°C, and melting point of the glass substrate is 975°C. When an amorphous semiconductor film was formed on this glass substrate and then placed in the atmosphere at 600°C, for 20 hours, a contraction in the substrate could be observed. However, any transfiguration that would affect the processes of manufacturing a semiconductor device was not recognized in the  
10 substrate. The 20-hour heating time, however, was too long for a mass production line.

[0006]

In order to solve the problems as described above, a new crystallization method was devised. Details of this method are described in Japanese Patent Application Laid-open Hei 7-183540. Here, this method will be briefly described. First, a minute amount of elements  
15 like nickel, palladium or lead is doped to an amorphous semiconductor film. For the doping process, a plasma CVD method, a vapor deposition method, an ion implantation method, a sputtering method, a solution applying method or the like may be performed. After the doping process, when the amorphous semiconductor film is placed in a nitrogen atmosphere at 550°C for 4 hours, for example, a crystalline semiconductor film with good characteristics can be  
20 obtained. Incidentally, the heating temperature and time most suitable for crystallization depends on the doping amount of the element and the states of the amorphous semiconductor film.

[0007]

The above was a description about the method of crystallizing the amorphous  
25 semiconductor film by heating. Meanwhile, since crystallization by laser annealing can impart high energy to the amorphous semiconductor film alone without excessively increasing the temperature of the substrate, it can also be employed for a plastic substrate or the like as well as a glass substrate having a low strain point.

[0008]

30 Furthermore, a method of performing laser annealing is one in which a laser beam emitted from a pulse oscillation type excimer laser, which is large in output, is processed by an optical system so that the laser beam thereof becomes a linear shape that is 10 cm or longer or a square spot that is several cm square at an irradiated surface to thereby make the laser beam scan (or relatively move the irradiation position of the laser beam to the irradiated surface).  
35 Because this method is high in productivity and industrially excellent, it is being preferably

employed.

[0009]

Different from when using a spot shape laser beam which requires a front, back, left, and right scan, when using the linear laser beam, in particular, the entire irradiated surface can be irradiated by the laser beam which requires only scanning at right angles in a longitudinal direction of the linear laser beam, resulting in high productivity. To scan in a direction at right angles to the linear direction is the most effective scanning direction. Because of the high productivity, using the laser beam that is emitted from the pulse oscillation type excimer laser and processed into a linear laser beam by an appropriate optical system for laser annealing at present prevails as a manufacturing technique for a liquid crystal display device using TFT.

[0010]

Further, there is also a method of crystallizing the amorphous semiconductor film by heat treatment and then further crystallizing the resultant film by laser annealing. With this method, the characteristics of the semiconductor film can be improved more than in the case where crystallization is performed either by heat treatment or laser annealing. In this method, in order to obtain the good characteristics, it is necessary to optimize conditions of both heat treatment and laser annealing. Manufacturing a thin film transistor (TFT) using the crystalline semiconductor film obtained by the above-mentioned method greatly improves the electrical characteristics of the TFT.

[0011]

[Problem to be Solved by the Invention]

However, since the crystallization method by means of laser beam irradiation can impart high energy to the semiconductor film without excessively increasing the temperature of the substrate, an abrupt temperature gradient is produced between the substrate and the semiconductor film. Consequently, the semiconductor film strains under a tensile stress.

[0012]

In addition, the semiconductor film becomes more compact by crystallization. This phenomenon can be confirmed from a decrease in thickness of the film. As described above, the semiconductor film contracts by crystallization, and that becomes a factor for bringing about strain in the film.

[0013]

These strains can also be observed by conducting Raman scattering spectroscopy, and thereby detecting a shift of the peak in the Raman spectrum after the laser beam irradiation.

[0014]

When a strain exist on a substrate of a semiconductor with insulated gate,

a potential barrier or trapping levels resulting from the strain of the semiconductor film are induced, which leads to a higher interface level between an active layer and a gate insulating film. Further, when the semiconductor film is strained, uniform application of an electric field cannot be performed, which leads to a malfunction of the semiconductor device. In addition, the strain in the surface of the semiconductor film impairs the flatness of the gate insulating film deposited by the sputtering method or the CVD method, and causes faulty insulation or the like, thereby reducing reliability. A surface scattering effect is pointed out as one of the factors for determining the TFT's field effect mobility. The flatness of the interface between the active layer and the gate insulating film of the TFT greatly affects the field effect mobility. The flatter the interface is, the lesser the TFT is not affected by scattering, so that high field effect mobility can be obtained. In this way, the strain in the semiconductor film affects all the characteristics of the TFT, thereby changing even production yields.

[0015]

The object of the present invention is to provide a method of forming a semiconductor film with little strain and then manufacturing a semiconductor device that uses the semiconductor film.

[0016]

[Means for Solving the Problem]

The present invention is characterized in that, after laser crystallization is performed on a semiconductor film that has been partially crystallized by first heat treatment, second heat treatment is carried out, whereby a strain formed by laser beam irradiation is lessened. As already described, laser beam irradiation forms a strain in the semiconductor film. (Fig. 1(B)) When the heating treatment is performed thereafter, the semiconductor film already heated at a high temperature hardly transforms. However, since a substrate is exposed to the highest temperature of all the processes carried out so far, it contracts. (Fig. 1(C)) The strain in the semiconductor film, resulting from laser beam irradiation can thus be lessened, so that the physical properties of the semiconductor film can be improved.

[0017]

The method of manufacturing a semiconductor device according to the present invention comprises the steps of: adding a metal element into an amorphous semiconductor film and carrying out the first heat treatment; irradiating a laser beam onto the amorphous semiconductor film to form a crystalline semiconductor film; and carrying out second heat treatment to reduce the strain in the crystalline semiconductor film formed by radiation of the laser beam.

[0018]

In the manufacturing method described above, the first and the second heat treatment is a thermal annealing method that uses an annealing furnace or an RTA method.

[0019]

5 The RTA method is the method of heating the substrate rapidly with a lamp to carry out heat treatment in a short time. In this specification, light radiated from the lamp is referred to as lamp light. The lamp light is radiated from the upper and/or lower side of the substrate. Further, the lamp light is the light radiated from a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp.

[0020]

10 Further, in the manufacturing method is characterized in that the heating temperature of the second heat treatment is higher than that of the first heat treatment. With this arrangement, the substrate is exposed to the highest temperature of all the processes carried out so far, so that the substrate contracts. For this reason, the strain formed by laser beam irradiation can be lessened.

15 [0021]

Note that, in the manufacturing method described above, the heating time of the second heat treatment is from one to 30 minutes.

[0022]

20 Moreover, in the manufacturing method, the metal element is one or a plurality of the elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au, Sn and Sb.

[0023]

[Embodiment Modes of the Invention]

Embodiment modes of the invention are explained using Fig.1.

25 [0024]

First, an insulating substrate (not shown) is formed on a substrate 10. A glass substrate or a quartz substrate having translucency is employed as the substrate 10. As the insulating substrate, an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed. The structure of the insulating substrate is not limited to a single layer. Lamination structure of at least two layers of the insulating films may also be employed. Note that, the insulating substrate may not be necessarily formed. Note that, the insulating substrate may not be formed.

[0025]

Next, a semiconductor film 11 is formed on the insulating substrate. (Fig. 1(A)) The

semiconductor film 11 is formed by using known means (a sputtering method, an LPCVD method or a plasma CVD method and the like) to form the semiconductor film having the amorphous structure. The semiconductor film 12 is formed to have a thickness of 25 to 80nm (preferably 30 to 60nm). Any material can be used for the semiconductor film. However, preferably, silicon or an alloy of silicon and germanium (SiGe) is employed.

[0026]

Thereafter, a metal element for promoting crystallization is added by using the known means such as the sputtering method or the solution applying method to form a metal containing layer 12. As the metal element, one or a plurality of metal elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au, Sn and Sb are employed.

[0027]

Then, the first heat treatment is carried out to partially crystallize the semiconductor film to thereby form a first crystalline semiconductor film 13. (Fig. 1(B)) Thermal annealing using the annealing furnace or the RTA method may be employed as the heat treatment.

[0028]

Then, the crystalline semiconductor film 15 is formed by laser crystallization. (Fig. 1(C)) The crystalline semiconductor film 15 that has contracted under the tensile stress 14 by laser irradiation is formed. Note that, it is preferable that, before laser crystallization, hydrogen contained in the semiconductor film is released. When heat treatment is carried out for approximately one hour at 400°C to 500°C to reduce the amount of contained hydrogen to 5% or less of the total number of atoms contained in the semiconductor film and then crystallization is performed, the surface of the film can be prevented from becoming rough. Generally, when the amorphous semiconductor film is formed by the sputtering method or the LPCVD method, the film contains a lower concentration of hydrogen than the amorphous semiconductor film formed by the plasma CVD method. Further, it is known that even the amorphous semiconductor film formed by the plasma CVD method has a low concentration of hydrogen if formed at 400°C or higher.

[0029]

In the laser crystallization method, an excimer laser, YAG laser, YVO<sub>4</sub> laser, YAlO<sub>3</sub> laser or YLF laser of a pulse oscillation type or a continuous emission type can be employed. When using these lasers, it is efficient to converge laser beams radiated from a laser oscillator into a linear form by means of an optical system and then irradiate the converged beam onto the semiconductor film. Crystallization conditions should be selected by an operator fitly. When using the excimer laser, the pulse oscillation frequency should be 300 Hz, and the laser energy density should be 100 to 800 mJ/cm<sup>2</sup> (typically 200 to 700 mJ/cm<sup>2</sup>). When using the YAG

laser, the second harmonic emitted from the YAG laser is used. Then, the pulse oscillation frequency should be one to 300 Hz, and the laser energy density should be 300 to 1000 mJ/cm<sup>2</sup> (typically 350 to 800 mJ/cm<sup>2</sup>). Then, the laser beams that have been converged into the linear form with their width of 100 to 1000μm, for example, 400μm should be irradiated onto the entire substrate surface. In this case, laser beam irradiation may also be performed with 50 - 98% overlap ratio of the beams that have been converged into the linear form.

[0030]

Further, laser crystallization can be performed in the air, in the atmosphere of an inert gas such as nitrogen, or in a reduced pressure atmosphere.

10 [0031]

Next, a second heat treatment by thermal annealing using the annealing furnace or the RTA method is carried out. (Fig. 1((D))) Thermal annealing using the annealing furnace should be performed for one to 30 minutes at a temperature higher than the first heat treatment. When using the RTA method, in the nitrogen atmosphere, for example, the heat treatment is carried out with 11 (infrared) halogen lamps 15 turned on: 11 of them are provided under the substrate and 10 of them are provided over the substrate. In the RTA method, a momentary increase in temperature is possible. However, temperature control may also be performed with a temperature rising rate or temperature lowering rate of 30 to 300°C per minute. The heat supplied from the halogen lamps (measured by a thermocouple embedded in a silicon wafer) is in the temperature range of 700 to 1300°C. However, optimum heat treatment conditions differ depending on the states of the substrate and the semiconductor film. Therefore, the operator should determine the optimum heat treatment conditions fitly.

[0032]

In this embodiment mode, the heat treatment was carried out in the nitrogen atmosphere. However, the inert gas such as helium (He), neon (Ne), or argon (Ar) may also be employed. The halogen lamps were herein used as a light source. However, it is also preferable to employ an ultraviolet lamp such as a xenon lamp as the light source.

[0033]

A heat treatment causes the substrate to contract in a direction indicated in reference numeral 18. Thus, contraction of the semiconductor film resulting from laser beam irradiation is lessened.

[0034]

Then, patterning is performed to form a semiconductor layer 20 of a desired shape. Thereafter, if TFTs are manufactured by using the semiconductor layer thus obtained, their electrical characteristics will be excellent.

[0035]

A more detailed description of the present invention framed as above will be given with the embodiments below.

[0036]

5 [Embodiments]

[Embodiment 1]

The embodiments of the present invention will be described with reference to Fig. 1

[0037]

10 First, an insulating substrate (not shown) is formed on a substrate 10. A glass substrate or a quartz substrate having translucency is employed as the substrate 10. As the insulating substrate, an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon oxynitride film is formed. The structure of the insulating substrate is not limited to a single layer. Lamination structure of at least two layers of the insulating films may also be employed. Further, the insulating substrate may not be formed. Further, the insulating  
15 substrate may not be formed. In this embodiment, the glass substrate is employed, and the silicon oxynitride film (not shown) having a film thickness of 150nm is formed on the glass substrate by the plasma CVD method.

[0038]

20 Next, a semiconductor film 11 is formed on the insulating substrate. (Fig. 1(A)) The semiconductor film 11 is formed by depositing the amorphous semiconductor film using the well-known means (a sputtering method, an LPCVD method or a plasma CVD method). This semiconductor film 12 is formed to have a thickness of 25 to 80nm (preferably 30 to 60nm). Any material can be used for the semiconductor film. However, preferably, silicon or an alloy of silicon and germanium (SiGe) is employed. In this embodiment, the amorphous silicon film  
25 having a film thickness of 55nm is formed at a temperature of 400°C by the plasma CVD method.

[0039]

Thereafter, a metal element for promoting crystallization is added by using the known means such as a sputtering method or a solution applying method to form the metal containing  
30 layer 12. As the metal element, one or a plurality of metal elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au, Sn and Sb are employed. In this embodiment, a solution that contains nickel is applied to the amorphous silicon film by a spin coating method.

[0040]

35 Then, the first heat treatment is carried out to partially crystallize the semiconductor

film to form the first crystalline semiconductor film 13. (Fig. 1(B)) Thermal annealing that uses the annealing furnace or the RTA method may be used for the heat treatment. In this embodiment, the heat treatment is carried out for 4 hours at a temperature of 550°C in the nitrogen atmosphere, using the annealing furnace.

5 [0041]

Then, a second crystalline semiconductor film 15 is formed by laser crystallization. (Fig. 1(C)) The crystalline semiconductor film 15 that has contracted under the tensile stress 14 by laser irradiation is formed. In this embodiment, the beams of the excimer laser are shaped by the optical system so as to produce the linear form on the irradiated surface, and laser  
10 beam irradiation is performed in the air. With this arrangement, crystallinity of the semiconductor film is improved. However, the crystalline semiconductor film 15 that has contracted by laser beam irradiation is formed.

[0042]

Then, the second heat treatment by thermal annealing using the annealing furnace or  
15 the RTA method is carried out. (Fig. 1(D)) In this embodiment, the RTA method is employed. The heat treatment is carried out for 5 minutes at a temperature of 750°C in the nitrogen atmosphere, using halogen lamps.

[0043]

This heat treatment causes the substrate to contract in the direction indicated by  
20 reference numeral 18. For this reason, contraction of the semiconductor film 13 resulting from laser beam irradiation is lessened.

[0044]

Then, patterning is performed to form the semiconductor layer 20 of a desired shape. If TFTs are then manufactured by using the semiconductor layer thus obtained, their electrical  
25 characteristics will be excellent.

[0045]

[Embodiment 2]

In this embodiment, a method of reducing a strain in the semiconductor film through the manufacturing process different from the process according to Embodiment 1 will be  
30 described with reference to Fig. 2.

[0046]

First, the state illustrated in Fig. 1(A) is obtained according to Embodiment 1.

[0047]

Then, the first heat treatment is carried out to partially crystallize the semiconductor

film to form the first crystalline semiconductor film 13. (Fig. 2(B)) Thermal annealing that uses the annealing furnace or the RTA method may be used for the heat treatment. In this embodiment, the heat treatment is carried out for 100 seconds at a temperature of 700°C in the nitrogen atmosphere, using the RTA method.

5 [0048]

Then, the crystalline semiconductor film is formed by laser crystallization. In this embodiment, the second harmonic emitted from the YAG laser is shaped by the optical system to produce the linear form on the irradiation plane, and laser beam irradiation is carried out in the nitrogen atmosphere. With this arrangement, crystallinity of the semiconductor film is improved. However, the semiconductor film 13 that has contracted due to laser beam irradiation is formed.

[0049]

Then, patterning is performed to form a semiconductor layer 21.

[0050]

15 Next, the second heat treatment by thermal annealing using the annealing furnace or the RTA method is carried out. The second heat treatment is carried out at a temperature higher than the first heat treatment. In this embodiment, thermal annealing using the annealing furnace is applied. And the heat treatment is carried out for 30 minutes at a temperature of 600°C in the nitrogen atmosphere.

20 [0051]

Since this heat treatment causes the substrate to contract in the direction indicated by reference numeral 18, contraction of the semiconductor film resulting from laser beam irradiation is lessened. Then, if TFTs are manufactured by using a semiconductor described above, their electrical characteristics will be excellent.

25 [0052]

[Embodiment 3]

In this embodiment, a method of lessening a strain of the semiconductor film by means of the heat treatment through the manufacturing process different from the process according to Embodiments 1 and 2 will be described with reference to Fig. 3.

30 [0053]

First, the glass substrate or the quartz substrate having translucency is employed as the substrate 10. In this embodiment, the glass substrate is used as the substrate 10.

[0054]

A conductive film is deposited over the substrate 10, and then etching is performed to

form a conductive film 31 of a desired shape. Any material having heat resistance can be used for the conductive film. An element selected from Ta, W, Ti, Mo, Cu, Cr and Nd, may be used. Alternatively, an alloy material or a compound material mainly consisting of the elements above may also be used. Alternatively, a semiconductor film represented by a crystalline silicon film doped with an impurity element such as phosphorus may also be employed. Still alternatively, an AgPdCu alloy may also be employed. Naturally, the structure of the conductive film is not limited to a single layer. Lamination of the layers of the conductive films may also be employed. In this embodiment, the conductive film 21 that comprises a W film having a thickness of 400nm is formed.

10 [0055]

Then, as an insulating film 32 formed on the conductive film 31, an insulating film such as the silicon oxide film, silicon nitride film, or silicon oxynitride film is formed. In this embodiment, the silicon oxide film having a thickness of 150nm is formed by the plasma CVD method.

15 [0056]

A semiconductor film 33 is formed on the insulating film. The semiconductor film 33 is formed by depositing the amorphous semiconductor film using the known means (the sputtering method, LPCVD method or plasma CVD method). The semiconductor film 23 is formed to have a thickness of 25 to 80nm (preferably 30 to 60nm). Any material can be used for the semiconductor film. However, preferably, silicon or the alloy of silicon and germanium (SiGe) is employed. In this embodiment, the amorphous silicon film having a film thickness of 55nm is formed by the plasma CVD method.

[0057]

Thereafter, a metal element for promoting crystallization is added by using the known means such as a sputtering method or a solution applying method to form the metal containing layer 34. (Fig. 3(A)) As the metal element, one or a plurality of metal elements selected from the group consisting of Fe, Co, Ni, Ru, Rh, Pd, Os, Ir, Pt, Cu, Ag, Au, Sn and Sb are employed. In this embodiment, a metal containing layer that contains nickel is formed by a sputtering method in the nitrogen atmosphere.

30 [0058]

Then, the first heat treatment is carried out to partially crystallize the semiconductor film to form the first crystalline semiconductor film 35. (Fig. 3(B)) Thermal annealing that uses the annealing furnace or the RTA method may be used for the heat treatment. In this embodiment, the heat treatment is carried out for 4 hours at a temperature of 550°C in the nitrogen atmosphere, using the annealing furnace.

[0059]

Then, a second crystalline semiconductor film 36 is formed by laser crystallization. (Fig. 3(C)) The crystalline semiconductor film 36 that has contracted under the tensile stress 14 by laser irradiation is formed. In this embodiment, the beams of the excimer laser are shaped by the optical system so as to produce the linear form on the irradiated surface, and laser beam irradiation is performed in the air. With this arrangement, crystallinity of the semiconductor film is improved. However, the crystalline semiconductor film 36 that has contracted by laser beam irradiation is formed.

[0060]

Then, the second heat treatment by thermal annealing using the annealing furnace or the RTA method is carried out. (Fig. 3(D)) In this embodiment, the RTA method is employed. The heat treatment is carried out for 4 minutes at a temperature of 700°C in the nitrogen atmosphere, using halogen lamps. The strain of the semiconductor film through suchlike heat treatment is lessened compared with that through a laser beam irradiation.

[0061]

Thereafter, patterning is performed to form the semiconductor layer 38 of a desired shape. If TFTs are then manufactured by using the semiconductor layer thus obtained, their electrical characteristics will be excellent.

[0062]

[Embodiment 4]

In this embodiment, the manufacturing method of an active matrix substrate is explained using Figs. 4 to 8. In this specification, a substrate on which both a driver circuit and a pixel portion are formed is referred to as an active matrix substrate expediently.

[0063]

First, in this embodiment, a substrate 320 is used, which is made of glass such as barium borosilicate glass or aluminum borosilicate, represented by such as Corning #7059 glass and #1737 glass. Note that, as the substrate 320, a quartz substrate, a silicon substrate, a metallic substrate or a stainless substrate on which is formed an insulating film. A plastic substrate with heat resistance to a process temperature of this embodiment may also be used.

[0064]

Then, a base film 321 formed of an insulating film such as a silicon oxide film, a silicon nitride film or a silicon oxynitride film is formed on the substrate 320. In this embodiment, a two-layer structure is used as the base film 321. However, a single-layer film or a layered structure consisting of two or more layers of the insulating film may be used. As a first layer of the base film 321, a silicon oxynitride film 321a is formed with a thickness of 10 to

200nm (preferably 50 to 100nm) with a plasma CVD method using  $\text{SiH}_4$ ,  $\text{NH}_3$ , and  $\text{N}_2\text{O}$  as reactive gas. In this embodiment, the silicon oxynitride film 321a (composition ratio Si = 32%, O = 27%, N = 24% and H = 17%) with a film thickness of 50nm is formed. Then, as a second layer of the base film 301, a silicon oxynitride film 321b is formed and laminated into a thickness of 50 to 200nm (preferably 100 to 150nm) with a plasma CVD method using  $\text{SiH}_4$  and  $\text{N}_2\text{O}$  as reaction gas. In this embodiment, the silicon oxynitride film 321b (composition ratio Si = 32%, O = 59%, N = 7% and H = 2%) with a film thickness of 100nm is formed.

[0065]

Subsequently, semiconductor film 322 is formed on the base film. The semiconductor film 322 is formed from a semiconductor film with an amorphous structure which is formed by a known method (such as a sputtering method, an LPCVD method, or a plasma CVD method) into the thickness of from 25 to 80nm (preferably 30 to 60nm). The material of the crystalline semiconductor film is not limited, but it is preferable to be formed of silicon, a silicon germanium (SiGe) alloy, or the like. Then, a first heat treatment is performed by thermal annealing to form a first crystalline region. In this embodiment, the metal containing layer 323 is formed by applying nickel using a solution applying method. For the first heat treatment, the metal containing layer 323 is exposed to nitrogen atmosphere at 575°C for 4 hours.

[0066]

Then, a laser crystallization is carried out. A crystalline semiconductor film 325 that has contracted under the tensile stress by laser beam irradiation is formed. In this embodiment, the second harmonic emitted from the YAG laser is shaped by the optical system so as to produce the linear form on the irradiated surface, and the laser beam irradiation is performed in the nitrogen atmosphere. (Fig. 4(C))

[0067]

To decrease the strain formed by irradiating the laser beam, a second heat treatment is conducted. In this embodiment, a lamp light is applied. In this embodiment, the semiconductor film is exposed to the nitrogen atmosphere at 700°C for 5 minutes using halogen lamp. The strain of the semiconductor film through suchlike heat treatment is lessened compared with after the laser crystallization.

[0068]

Thus formed crystalline semiconductor film is patterned into the desired shape to form the semiconductor layers 402 to 406.

[0069]

After the formation of the semiconductor layer 402 to 406, a minute amount of

impurity element (boron or phosphorus) may be doped to control the threshold of the TFT.

[0070]

Then, a gate insulating film 407 is then formed for covering the semiconductor layers 402 to 406. The gate insulating film 407 is formed of an insulating film containing silicon by a plasma CVD method or a sputtering method into a film thickness of from 40 to 150nm. In this embodiment, the gate insulating film 407 is formed of a silicon oxynitride film into a thickness of 110nm by a plasma CVD method (composition ratio Si = 32%, O = 59%, N = 7%, and H = 2%). Naturally, the gate insulating film is not limited to the silicon oxynitride film, and other insulating films containing silicon may be used as a single layer or a layered structure.

[0071]

Further, when the silicon oxide film is used, it is possible to be formed by a plasma CVD method in which TEOS (TEtraethyl OrthoSilicate) and O<sub>2</sub> are mixed and discharged at a high frequency (13.56 MHz) power density of 0.5 to 0.8 W/cm<sup>2</sup> with a reaction pressure of 40 Pa and a substrate temperature of 300 to 400°C. Good characteristics as the gate insulating film can be obtained in thus manufactured silicon oxide film by subsequent thermal annealing at 400 to 500°C.

[0072]

Then, as shown in Fig. 5(A), on the gate insulating film 407, a first conductive film 408 with a thickness of 20 to 100nm and a second conductive film 409 with a thickness of 100 to 400nm are formed and laminated. In this embodiment, the first conductive film 408 of TaN film with a film thickness of 30nm and the second conductive film 409 of a W film with a film thickness of 370nm are formed into lamination. The TaN film is formed by sputtering with a Ta target under a nitrogen containing atmosphere. Besides, the W film is formed by the sputtering method with a W target. The W film may also be formed by a thermal CVD method using tungsten hexafluoride (WF<sub>6</sub>). Whichever method is used, it is necessary to make the material have low resistance to be used as a gate electrode, and it is preferable that the resistivity of the W film is set to less than or equal to 20 μΩcm. By making the crystal grains large, it is possible to make the W film have lower resistivity. However, in the case where many impurity elements such as oxygen are contained within the W film, crystallization is inhibited and the resistivity becomes higher. Therefore, in this embodiment, by forming the W film by a sputtering method using a W target with a high purity (99.9999%) and in addition, by paying sufficient attention to prevent impurities within the gas phase from mixing therein during the film formation, a resistivity from 9 to 20 μΩcm can be realized.

[0073]

Note that, in this embodiment, the first conductive film 408 is made of TaN, and the

second conductive film 409 is made of W, but the material is not particularly limited thereto, and either film may be formed of an element selected from the group consisting of Ta, W, Ti, Mo, Al, Cu, Cr, and Nd, or an alloy material or a compound material containing the above element as its main constituent. Besides, a semiconductor film, typified by a crystalline silicon  
5 film doped with an impurity element such as phosphorus, may be used. Further, an AgPdCu alloy may be used. Furthermore, any combination may be employed such as a combination in which the first conductive film is formed of tantalum (Ta) and the second conductive film is formed of W, a combination in which the first conductive film is formed of titanium nitride (TiN) and the second conductive film is formed of W, a combination in which the first  
10 conductive film is formed of tantalum nitride (Ta<sub>N</sub>) and the second conductive film is formed of Al, or a combination in which the first conductive film is formed of tantalum nitride (Ta<sub>N</sub>) and the second conductive film is formed of Cu.

[0074]

Next, resist masks 410 to 415 are formed using a photolithography method, and a first  
15 etching process is performed in order to form electrodes and wirings. This first etching process is performed with the first and second etching conditions. In this embodiment, as the first etching conditions, an ICP (Inductively Coupled Plasma) etching method is used, a gas mixture of CF<sub>4</sub>, Cl<sub>2</sub> and O<sub>2</sub> is used as etching gas, the gas flow rate is set to 25/25/10 (sccm) each, and plasma is generated by applying a 500 W RF (13.56 MHz) power to a coil shape electrode under  
20 the pressure of 1 Pa. A dry etching device with ICP (Model E645- ICP) produced by Matsushita Electric Industrial Co. Ltd. is used here. A 150 W RF (13.56 MHz) power is also applied to the substrate side (sample stage) to apply a negative self-bias voltage substantially. The W film is etched with the first etching conditions, and the end portion of the first conductive layer is formed into a tapered shape.

25 [0075]

Thereafter, the resist masks 410 to 415 are changed into the second etching conditions without being removed, a mixed gas of CF<sub>4</sub> and Cl<sub>2</sub> is used as an etching gas, the gas flow rate is set to 30/30 (sccm) each, and plasma is generated by applying a 500 W RF (13.56 MHz) power to a coil shape electrode under 1 Pa thereby to perform etching for about 30 seconds. A  
30 20 W RF (13.56 MHz) power is also applied substantially to the substrate side (sample stage) to a negative self-bias voltage. The W film and the Ta<sub>N</sub> film are both etched in the same degree under the second etching conditions in which CF<sub>4</sub> and Cl<sub>2</sub> are mixed. Note that, the etching time may be increased by approximately 10 to 20% in order to perform etching without any residue on the gate insulating film.

35 [0076]

In the first etching process, the end portions of the first and second conductive layers are formed to have a tapered shape due to the effect of the bias voltage applied to the substrate side by adopting resist masks with suitable shape. The angle of the tapered portions may be set to 15° to 45°. Thus, first shape conductive layers 417 to 422 (first conductive layers 417a to 422a and second conductive layers 417b to 422b) constituted of the first conductive layers and the second conductive layers are formed by the first etching process. Reference numeral 416 denotes a gate insulating film, and regions of the gate insulating film which are not covered by the first shape conductive layers 417 to 422 are made thinner by approximately 20 to 50nm by etching.

10 [0067]

Then, a first doping process is performed without removing resist masks (Fig. 5(C)). Doping may be carried out by an ion doping method or an ion implantation method. The condition of the ion doping method is that a dosage is  $1 \times 10^{13}$  to  $5 \times 10^{15}$  atoms/cm<sup>2</sup>, and an acceleration voltage is 60 to 100 keV. In this embodiment, the dosage is  $1.5 \times 10^{15}$  atoms/cm<sup>2</sup> and the acceleration voltage is 80 keV. As the impurity element for imparting the n-type conductivity, an element belonging to group 15 of the periodic table, typically phosphorus (P) or arsenic (As) is used, and phosphorus is used here. In this case, the conductive layers 417 to 421 become masks to the impurity element for imparting the n-type conductivity, and high concentration impurity regions 306 to 310 are formed in a self aligned manner. The impurity element for imparting the n-type conductivity is added to the high concentration impurity regions 306 to 310 in the concentration range of  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>.

20 [0078]

Thereafter, a second etching process is performed without removing the resist masks. A mixed gas of CF<sub>4</sub>, Cl<sub>2</sub> and O<sub>2</sub> may be used as etching gas and the W film is selectively etched. Then, the second conductive layers 428b to 433b are formed by a second etching process. On the other hand, the first conductive layers 417a to 422a are hardly etched, and the second shape conductive layers 428 to 433 are formed.

[0079]

Next, a second doping process is performed as shown in Fig. 6(A) without removing the masks from resists. The impurity element which imparts n-type conductivity is doped under the condition that the dose amount is lower than that of a first doping process with an acceleration voltage 70 to 120 keV. In this embodiment, the dosage is  $1.5 \times 10^{14}$  atoms/cm<sup>2</sup>, and the acceleration voltage is 90 keV. In the second doping process a second shaped conductive layers 428 to 433 are used as masks, and the impurity elements are doped with a semiconductor layer at the below of the second conductive layers 428b to 433b. Second high

concentration impurity regions 423a to 427a and low concentration impurity region 423b to 427b are newly formed.

[0080]

Next, after the resist masks are removed, masks 434a and 434b are newly formed, and  
5 the third etching process is performed as shown in Fig. 6(B). A mixed gas of SF<sub>6</sub> and Cl<sub>2</sub> is  
used as an etching gas, the gas flow rate is set to 50/10 (sccm), and plasma is generated by  
applying a 500 W RF (13.56 MHz) power to a coil shape electrode under the pressure of 1.3 Pa  
to thereby perform etching for about 30 seconds. A 10 W RF (13.56 MHz) power is applied to  
the substrate side (sample stage) to apply a negative self-bias voltage substantially. Thus, the  
10 third shape conductive layers 435 to 438 are formed by etching the TaN film of the p-channel  
type TFT and the TFT of the pixel portion (pixel TFT) by means of the third etching process  
mentioned above.

[0081]

Next, after removing the resist masks, the insulating layers 439 to 444 are formed by  
15 removing the gate insulating film 416 selectively using the second shape conductive layer 428  
and 430, and the second shape conductive layers 435 to 438 as masks. (Fig. 6(C))

[0082]

Subsequently, other resist masks 445a to 445c are formed and a third doping process is  
carried out. By the third doping process, there are formed impurity regions 446 and 447 added  
20 with impurity elements for providing a conductivity type reverse to the one conductivity type  
mentioned above at semiconductor layers constituting active layers of p-channel type TFTs.  
The impurity regions are formed in a self aligned manner by adding the impurity elements  
providing p-type by using the second conductive layers 435a and 438a as masks against the  
impurity elements. In this embodiment, the impurity regions 446 and 447 are formed by an ion  
25 doping process using diborane (B<sub>2</sub>H<sub>6</sub>) (Fig. 7(A)). In the third doping process, the  
semiconductor layers forming n-channel TFTs are covered by the resist masks 445a to 445c.  
Although the impurity regions 446 and 447 are added with phosphorus at concentrations  
different from each other by the first doping process and the second doping process, in  
whichever of the regions, by carrying out the doping processing such that the concentration of  
30 the impurity element for providing p-type falls in a range of  $2 \times 10^{20}$  to  $2 \times 10^{21}$  atoms/cm<sup>3</sup>, the  
impurity regions function as source regions and drain regions of p-channel TFTs and  
accordingly, no problem is posed. In this embodiment, portions of the semiconductor layers  
constituting active layers of p-channel TFTs are exposed and accordingly, there is achieved an  
advantage that the impurity element (boron) is easy to be added.

35 [0083]

The impurity regions are formed at the respective semiconductor layers thorough the above-described steps.

[0084]

Next, a first interlayer insulating film 461 is formed by removing the resist masks  
5 445a to 445c. The first interlayer insulating film 461 is formed by an insulating film including silicon and having a thickness of 100 through 200nm by using a plasma CVD process or a sputtering process. In this embodiment, a silicon oxynitride film having a film thickness of 150nm is formed by a plasma CVD process. Naturally, the first interlayer insulating film 461 is not limited to the silicon oxynitride film but other insulating film including silicon may be  
10 used as a single layer or a layered structure.

[0085]

Next, as shown by Fig. 7(B), by performing a heat treatment, the crystallinity of the semiconductor layers are recovered, and the impurity elements added to the respective semiconductor layers are activated. This heat treatment is carried out by a thermal annealing  
15 process using a furnace annealing furnace, a RTA process, a laser annealing method and the like. The thermal annealing method may be carried out in a nitrogen atmosphere having an oxygen concentration of 1 ppm or smaller, preferably .1 ppm or smaller at 400 through 700°C, typically, 500 to 550°C. A laser annealing method can be carried out by using the second harmonic of YAG laser and the like. In this embodiment, the activation process is carried out by a heat  
20 treatment at 550°C for 4 hours.

[0086]

Further, the heat treatment may be carried out before the first interlayer insulating film is formed. However, when a wiring material used is easily affected by heat, it is preferable to carry out the heat treatment after forming the interlayer insulating film (insulating film whose  
25 major component is silicon, for example, silicon nitride film) for protecting wirings as in this embodiment.

[0087]

Further, a hydrogenation will be possible by carrying out a heat treatment (at 300 to 550°C for 1 to 12 hours). This step is a step of terminating dangling bond of the  
30 semiconductor layer by hydrogen included in the first interlayer insulating film 461. The semiconductor layer can be hydrogenated irrespective of existence of the first interlayer insulating film. As other means of hydrogenation, plasma hydrogenation (using hydrogen excited by plasma), and a heat treatment in an atmosphere including 3 to 100% of hydrogen at 300 to 450°C for 1 to 12 hours.

35 [0088]

Next, a second interlayer insulating film 462 comprising an inorganic insulating material or an organic insulating material is formed on the first interlayer insulating film 461. In this embodiment, an acrylic resin film having film thickness of 1.6 $\mu$ m is used, which has a viscosity of 10 to 1000cp, preferably, 40 to 200cp and in which unevenness is formed at a surface thereof.

[0089]

In this embodiment, in order to prevent the specular reflection, unevenness is formed on the surfaces of the pixel electrodes by forming the second interlayer insulating film with unevenness on the surface. Also, in order to attain light scattering characteristics by forming the unevenness on the surfaces of the pixel electrodes, protrusions may be formed in regions below the pixel electrodes. In this case, since the same photomask is used in the formation of the TFTs, the protrusions can be formed without increasing the number of processes. Note that the protrusions may be provided suitably in the pixel portion region except for the wirings and the TFT portion on the substrate. Thus, the unevenness is formed on the surfaces of the pixel electrodes along the unevenness formed on the surface of the insulating film covering the protrusions.

[0090]

Also, a film with the surface planarized may be used as the second interlayer insulating film 462. In this case, after the formation of the pixel electrodes, unevenness is formed on the surface by adding a process using a known method such as a sandblast method or an etching method. Thus, since the specular reflection is prevented and reflection light is scattered, it is preferable whiteness degree be increased.

[0091]

Then, in a driver circuit 506, wirings 463 to 467 electrically connected to the respective impurity regions are formed. Note that, those wirings are formed by patterning a lamination film of a Ti film with a film thickness of 50nm and an alloy film (alloy film of Al and Ti) with a film thickness of 500nm. Naturally, not only the double structure, but the single layer structure or triple or more layered structure can be used. Further, the material of wiring is not limited to the Al and Ti. For example, wirings can be formed by patterning the laminated film in which Al and Cu are formed on a TaN film and further Ti film is formed.

[0092]

Also, in a pixel portion 507, a pixel electrode 470, a gate wiring 469, and a connection electrode 468 are formed (Fig. 7(C)). With this connection electrode 468, an electrical connection between a source wiring (lamination layer of 443b and 449) and the pixel TFT is formed. Also, an electrical connection between the gate wiring 469 and the gate electrode of

the pixel TFT is formed. With respect to the pixel electrode 470, an electrical connection with the drain region 442 of the pixel TFT 504 and an electrical connection with the semiconductor layer 458 which functions as one of electrodes for forming a storage capacitor are formed. It is desired that a material having a high reflectivity, such as a film containing Al or Ag as its main constituent, or a lamination film thereof, be used for the pixel electrode 470.

[0093]

Thus, the driver circuit 506 having a CMOS circuit formed of an n-channel TFT 501 and a p-channel TFT 502 and an n-channel TFT 503, and the pixel portion 507 having a pixel TFT 504 and a storage capacitor 505 can be formed over the same substrate. In this way, the active matrix substrate is completed.

[0094]

The n-channel type TFT 501 of the driver circuit 506 has a channel forming region 423c, a low concentration impurity region 423b (GOLD region) overlapping with the first conductive layer 428a constituting a portion of the gate electrode, and a high concentration impurity region 423a which functions as the source region or the drain region. The p-channel TFT 502 forming the CMOS circuit by connecting with the n-channel TFT 501 through an electrode 466 has a channel forming region 446d, an impurity region 446b and 446c formed outside the gate electrode, and a high concentration impurity region 446a which function as the source region or the drain region. The n-channel TFT 503 has a channel forming region 425c, a low concentration impurity region 425b (GOLD region) overlapping with the first conductive layer 430a comprising a part of the gate electrode, and a high concentration impurity region 425a which functions as the source region or the drain region.

[0095]

The pixel TFT 504 of the pixel portion includes a channel forming region 426c, a low concentration impurity region 426b (LDD region) formed outside the gate electrode, and the high concentration impurity region 426a functioning as a source region or a drain region. Besides, impurity elements imparting p-type conductivity are added to the respective semiconductor layers 447a and 447b functioning as one of the electrodes of the storage capacitor 505. The storage capacitor 505 is formed of the electrode 438 (a lamination of 438a and 438b) and the semiconductor layers 447a to 447c using the insulating film 444 as a dielectric material.

[0096]

Further, in the pixel structure of this embodiment, an end portion of the pixel electrode is formed by arranging it so as to overlap with the source wiring so that the gap between the pixel electrodes is shielded from light without using a black matrix.

[0097]

A top view of the pixel portion of the active matrix substrate manufactured in this embodiment is shown in Fig. 8. Note that, the same reference numerals are used to indicate parts corresponding Figs. 4 to 7. A dot-dashed line A-A' in Fig. 7(C) corresponds to a sectional view taken along the line A-A' in Fig. 8. Also, a dot-dashed line B-B' in Fig. 7(C) corresponds to a sectional view taken along the line B-B' in Fig. 8.

[0098]

This embodiment can be performed by freely combining with any one of Embodiments 1 to 3.

10 [0099]

[Embodiment 5]

In this embodiment, an explanation will be given as follows of steps of fabricating a reflection type liquid crystal display device from the active matrix substrate fabricated in Embodiment 4. Fig. 9 is used for explanation.

15 [0100]

First, in accordance with Embodiment 4, there is provided the active matrix substrate in the state of Fig. 7(C) and thereafter, an orientation film 567 is formed above the active matrix substrate of Fig. 7(C) at least above the pixel electrode 470, and a rubbing process is carried out. Further, in this embodiment, before forming the orientation film 567, by patterning an organic resin film such as an acrylic resin film, columnar spacers 572 are formed at desired positions in order to retain an interval between substrates. Further, in place of the columnar spacers, ball-shaped spacers may be scattered over an entire face of the substrate.

[0101]

25 Next, a counter substrate 569 is prepared. Subsequently, there are formed color layers 570 and 571 and a leveling film 573. A light shielding portion is formed by overlapping the color layer 570 of red color and the color layer 572 of blue color. Further, the light shielding portion may be formed by overlapping portions of a color layer of red color and a color layer of green color.

[0102]

30 In this embodiment, there is used the substrate shown in Embodiment 4. Therefore, in Fig. 8 showing the top view of the pixel portion of Embodiment 4, it is necessary to shield at least a gap between the gate wiring 469 and the pixel electrode 470, a gap between the gate wiring 469 and the connection electrode 468 and a gap between the connection electrode 468 and the pixel electrode 470. In this embodiment, the respective color layers are arranged such that the light shielding portions constituted by laminating the color layers overlap positions to

35

be shielded and the counter substrate is pasted thereto.

[0103]

Thus, a number of steps can be reduced by shielding the gaps between the respective pixels with the light shielding portions constituted by laminating the color layers without  
5 forming light shielding layers such as black masks.

[0104]

Next, the counter electrode 576 constituted with a transparent conductive film is  
—formed on the leveling film 573 at least on the pixel portion, an orientation film 574 is formed  
over an entire face of the counter substrate, and the rubbing process is carried out.

10 [0105]

Further, the active matrix substrate formed with the pixel portion and the drive circuit,  
and the counter substrate are pasted together by sealing member 568. The sealing member 568  
is mixed with fillers, and the two substrates are pasted together at a uniform interval  
therebetween by the fillers and columnar spacers. Thereafter, the interval between the two  
15 substrates is injected with a liquid crystal material 575 and is completely sealed by a sealant  
(not illustrated). A known liquid crystal material may be used for the liquid crystal material  
575. In this way, the reflection type liquid crystal display device shown in Fig. 9 is finished.  
Then, if necessary, the active matrix substrate or the counter substrate may be divided into a  
desired shape. Further, a polarizing plate (not illustrated) is pasted only to the counter  
20 substrate. Further, FPC is pasted thereto by using known technique.

[0106]

The liquid crystal display panel fabricated as described above can be used as display  
portions of various electronic devices.

[0107]

25 Note that, this embodiment can be performed by freely combining with any one of  
Embodiments 1 to 4 or Embodiment 7.

[00108]

[Embodiment 6]

In this embodiment, the manufacturing process of an active matrix liquid crystal  
30 display device which is different from that in Embodiment 5 from the active matrix substrate  
manufactured in Embodiment 4 is described below. Fig. 10 is used for explanation.

[0109]

First, in accordance with Embodiment 4, the active matrix substrate in a state shown in  
Fig. 7(C) is obtained, and thereafter, an orientation film 1067 is formed on the active matrix

substrate of Fig. 7, and a rubbing process is performed thereon. Note that, in this embodiment, before the formation of the orientation film 1067, a columnar spacer for retaining a gap between the substrates is formed at a desired position by patterning an organic resin film such as an acrylic resin film. Further, spherical spacers may be scattered on the entire surface of the substrate in place of the columnar spacer.

[0110]

Next, a counter substrate 1068 is prepared. On the counter substrate 1068, there are formed a color layer 1074, a light shielding layer 1075 and color filters arranged to correspond to the respective pixels. Further, the driver circuit portion is also provided with a light shielding layer 1077. A leveling film 1076 is provided to cover the color filters and the light shielding layer 1077. Next, in the pixel portion, a counter electrode 1069 formed from a transparent conductive film on the leveling film 1076, and an orientation film 1070 is formed on the entire surface of the counter substrate, and a rubbing process is conducted thereon.

[0111]

Then, the active matrix substrate on which a pixel portion and a driver circuit are formed is pasted to the counter substrate by a sealing member 1071. A filler is mixed into the sealing member 1071, and the two substrates are pasted together keeping a uniform gap by this filler and the columnar spacer. Thereafter, a liquid crystal material 1073 is injected between both the substrates to seal the substrates completely by a sealant (not shown). A known liquid crystal material may be used as the liquid crystal material 1073. Thus, the active matrix liquid crystal display device shown in Fig. 10 is completed. Then, if necessary, the active matrix substrate or the counter substrate is parted into a desired shape. In addition, by using a known technique, a polarizing plate or the like is suitably provided. Then, an FPC is stuck to the substrate using a known technique.

[0112]

The liquid crystal display panel manufactured in this way can be used as a display portion of various electronic devices.

[0113]

This embodiment can be performed by freely combining with any one of Embodiments 1 to 4 and Embodiment 7.

[0114]

[Embodiment 7]

In this embodiment, an active matrix substrate on which the structure of TFTs is different from that on the substrate manufactured according to Embodiment 4 is given as an example. An example of a light emitting device manufactured according to the present invention

will be described. In the present specification, a display panel in which light emitting elements formed on the substrate are encapsulated between the substrate and a covering material, and a display module mounted with an IC on the display panel are collectively referred to as the light emitting device. Note that, the light emitting element comprises a light emitting layer  
5 containing an organic compound which emits electroluminescence by applying an electrical field, an anode layer, and a cathode layer. There are two types of the electroluminescence emitted from organic compounds: one is fluorescence which is light emission upon returning to the ground state and the other is phosphorescence which is light emission upon returning to the ground state from the triplet excited state. Here, the electroluminescence refers to either one or  
10 both types of the light emission described above.

[0115]

A driver circuit 605 comprising an n-channel TFT 601 and a p-channel TFT 602 and a pixel portion 606 comprising a switching TFT 603 and a current controlling TFT 604 are formed on an active matrix substrate shown in Fig. 11.

15 [0116]

These TFTs are manufactured by first forming a base film 611 over a substrate 610 and then providing a channel forming region, a source region, a drain region, an LDD region and the like in a semiconductor layer on the base film. The semiconductor layer is formed according to the present invention, as in Embodiments 1 through 5.

20 [0117]

Gate electrodes 628 to 633 formed on a gate insulating film 612 respectively form a layered structure comprising first conductive layers and second conductive layer. They are characterized in that the ends thereof are tapered. This tapered shape is formed by performing etching at least three times. By taking advantage of the shape of a gate electrode formed by each  
25 etching process, impurities are introduced into the semiconductor layer.

[0118]

Specifically, first gate electrodes whose ends are tapered by performing a first etching process is used as masks, and first doping process is performed in a self-aligning manner, thereby forming a high concentration impurity region. Next, the second conductive layer is  
30 selectively etched to form second gate electrodes. A second doping process is then performed by using the tapered portions of the first conductive layer in the second gate electrodes to form a low concentration impurity region. Then, the tapered portions of the first conductive layer are partially etched to form third gate electrodes. At this point, an insulating film is also etched simultaneously to form an insulating film 621. Thereafter, n-channel TFTs and the pixel  
35 portion are masked to perform a third doping process. Through this third doping process is

formed an impurity region doped with an impurity element that imparts a conductivity opposite to the above-mentioned one conductivity to the semiconductor layer that becomes an active layer for p-channel TFTs.

[0119]

5           The LDD region formed by using the tapered portions of the second gate electrodes in the first conductive layer is provided to improve the reliability of the n-channel TFT. With this arrangement, deterioration of an on-state current resulting from a hot carrier effect is prevented. In the LDD region, by using an ion doping method, the ions of the impurity element are accelerated in the electric field. Then, the impurity element is introduced into the  
10 semiconductor film through the ends of the gate electrodes and the gate insulating film in the vicinity of the ends of the gate electrodes.

[0120]

          In this way, an LDD region 634 and a source region or drain region 639 are formed on the outside of a channel forming region 671 of the n-channel TFT 601. A part of the LDD  
15 region 634, which is indicated by reference numeral 634b, is formed so as to overlap with the gate electrode 628. A region 634a is not overlapped with the gate electrode 628. The p-channel TFT 602 has the same configuration, and comprises a channel forming region 657, LDD regions 656 and 657, and a source or drain region 655. In this embodiment, the TFTs take on a single-gate structure. However, they may take on a double-gate structure or a  
20 triple-gate structure instead.

[0121]

          The switching TFT 603 formed of an n-channel TFT takes on a multi-gate structure in order to reduce an off-state current. An LDD region 637 and a source or drain region 642 are provided on the outside of a channel forming region 674. In the current controlling TFT 604  
25 formed of a p-channel TFT, LDD regions 656 and 657, and a source or drain region 655 are provided on the outside of a channel forming region 672. In this embodiment, the current controlling TFT 604 takes on the single-gate structure. However, the current controlling TFT 604 may take on the double-gate structure or the triple-gate structure instead.

[0122]

30           Interlayer insulating films comprise a first interlayer insulating film 635 having a thickness of 50 to 500nm and a second interlayer insulating film 636. The first interlayer insulating film 635 is formed of an inorganic material such as silicon oxide, silicon nitride, or silicon oxynitride, and the second interlayer insulating film is formed of an organic insulating material such as polyimide, acrylic, polyimide amide, and BCB (benzocyclobutene). Forming  
35 the second interlayer insulating film of the organic insulating material in this manner allows the

surface of the film to be planarized well. Further, generally, the dielectric constant of organic resin materials is low, so that the parasitic capacitance of the semiconductor device can be reduced. However, organic resin materials have hygroscopicity, so that they are not suitable to be used as a protective film. Accordingly, it is preferable that the second interlayer insulating film 636 is used in combination with the first interlayer insulating film 635.

[0123]

Thereafter, a resist mask having a predetermined pattern is formed, and then contact holes that extend to the source regions or the drain regions formed on the respective semiconductor layers are formed. Formation of the contact holes is carried out by dry etching. In this case, a mixture of  $\text{CF}_4$ ,  $\text{O}_2$ , and He is used as an etching gas to first etch the second interlayer insulating film 636 formed of the organic resin material. Then,  $\text{CF}_4$  and  $\text{O}_2$  are used as the etching gas to etch the first interlayer insulating film 635.

[0124]

Then, a conductive-metal film is formed by sputtering or vacuum deposition method to form a resist mask with pattern. Thereafter, wirings 701 to 707 are formed by etching. In this way, an active matrix substrate can be formed.

[0125]

A light emitting device shown in Fig. 12 is manufactured by using the active matrix substrate in Fig. 11. Here, the wiring 706 is source wiring (corresponding to a current supply line) to the current controlling TFT. Reference numeral 707 denotes an electrode to be electrically connected to a pixel electrode 710 of the current controlling TFT by overlapping with the pixel electrode 710.

[0126]

Incidentally, reference numeral 710 is a pixel electrode (an anode for light emitting elements) formed of a transparent conductive film. A compound of indium oxide and tin oxide, a compound of indium oxide and zinc oxide, zinc oxide, tin oxide, or indium oxide can be employed for the transparent conductive film. Alternatively, the transparent conductive film doped with gallium may also be used. The pixel electrode 710 is formed on a flat interlayer insulating film 711 before the wirings described above are formed. In this embodiment, it is extremely important to level the step due to the TFTs by using the leveling film 711 formed of a resin. Since a light emitting layer to be formed later is very thin, the step sometimes cause faulty luminance. Accordingly, it is desirable to perform this flattening process before the pixel electrode is formed so as to allow the light emitting layer to be formed as flat as possible.

[0127]

After the wirings 701 to 707 are formed, a bank 712 is formed, as shown in Fig. 12.

The bank 712 may be formed by patterning an insulating film or an organic resin film having a thickness of 100 to 400nm and containing silicon.

[0128]

Since the bank 712 is an insulating film, care should be taken to avoid the electrostatic damage of elements at the time of formation of the bank. In this embodiment, the insulating film that forms the bank 712 is doped with carbon particles or metal particles to reduce resistivity, thereby suppressing generation of static electricity. At this time, the doping amount of the carbon particles or the metal particles should be adjusted so that the resistivity becomes  $1 \times 10^6$  to  $1 \times 10^{12} \Omega\text{m}$ , preferably from  $1 \times 10^8$  to  $1 \times 10^{10} \Omega\text{m}$ .

10 [0129]

A light emitting layer 713 is formed on the pixel electrode 710. Though the layer for a single pixel is illustrated in Fig. 12, light emitting layers corresponding to the respective colors of R (red), G (green), and B (blue) are formed separately in this embodiment. Further, in this embodiment, a low molecular organic light emitting material is formed by evaporation. Specifically, the light emitting layer 713 takes on a layered structure by forming a tris-8-quinolinolate aluminum ( $\text{Alq}_3$ ) complex film having a thickness of 70nm as a light emitting layer over a copper phthalocyanine (CuPc) film having a thickness of 20nm as a hole injecting layer. A light emission color can be controlled by adding a fluorescent pigment such as quinacridone, perylene, or DCM 1 to  $\text{Alq}_3$ .

20 [0130]

The materials described above are examples of organic light emitting materials that can be used for the light emitting layer, and the present invention is not limited to these materials. A light emitting layer, and a charge transporting layer or a charge injecting layer may be combined freely to form the light emitting layer (used for light emission and for causing carrier movement necessary for the light emission). For example in this embodiment, a case where a low molecular organic light emitting material is employed for the light emitting layer is described. However, a high molecular organic light emitting material may also be used. Further, an inorganic material such as silicon carbide can also be employed for the charge transporting layer or the charge injecting layer. A known material can be used for these organic light emitting material and inorganic material.

[0131]

Next, a cathode 714 comprising the conductive film is provided on the light emitting layer 713. In this embodiment, an alloy film of aluminum and lithium is used as the conductive film. Naturally, a known Mg-Ag film (an alloy film of magnesium and silver) may also be used. The conductive film made from an element belonging to Group 1 or Group 2 of

the periodic table or the conductive film doped with these elements should be employed for forming the cathode.

[0132]

Upon formation of the cathode 714, a light emitting element 715 is completed.

5 Herein, the light emitting element 715 refers to diodes that comprises the pixel electrode (anode) 710, the light emitting layer 713, and the cathode 714.

[0123]

It is effective to provide a passivation film 716 so as to completely cover the light emitting element 715. An insulating film including a carbon film, the silicon nitride film, or  
10 the silicon oxynitride film is used as the passivation film 716. A single layer of one of these films or lamination of these films is used.

[0134]

In this case, it is preferable that a film providing good coverage is used as the passivation film. It is effective to use a carbon film, especially a DLC (diamond-like carbon)  
15 film for this purpose. The DLC film can be formed in a temperature range of room temperature to 100°C or lower. Therefore, the DLC film can be readily formed even in a region above the light emitting layer 713 having a low heat resistance. Further, the DLC film has a high blocking effect against oxygen, so that oxidation of the light emitting layer 713 can be suppressed. For this reason, oxidation of the light emitting layer 713 during a subsequent  
20 sealing process can be prevented.

[0135]

Further, a sealant 717 is provided over the passivation film 716, and a covering material 718 is bonded together. An ultraviolet cured resin may be used for the sealant 717, and it is effective to provide therein a substance that has the effect of absorbing moisture or  
25 preventing oxidation. In this embodiment, the covering material 718 made by forming carbon films (preferably the diamond-like carbon films) over both sides of a glass substrate, quartz substrate, or plastic substrate (including a plastic film) is employed.

[0136]

In this way, the light emitting device having a structure as shown in Fig. 12 is  
30 completed. Incidentally, after formation of the bank 712, it is effective to continuously process steps up to formation of the passivation film 716, without exposure to the atmosphere by using a multi-chamber type film forming device (or an in-line type film forming device). Further, it is also possible to continuously process steps up to bonding the covering material 718 together without exposure to the atmosphere.

35 [0137]

In this way, the n-channel TFTs 601 and 602, the switching TFT (n-channel type TFT) 603, and the current controlling TFT (n-channel type TFT) 604 are formed over an insulating material 501 of the plastic substrate. The number of masks required in the manufacturing process up to this point is less than that required for a typical active matrix light emitting device.

5 [0138]

More specifically, the TFT manufacturing process is substantially simplified, so that improvement in production yields and reduction in manufacturing costs can be realized.

[0139]

Further, as described with reference to Fig. 12, an n-channel TFT that is resistant  
10 against deterioration resulting from the hot carrier effect can be formed by providing the impurity region which is superposed over the gate electrode is through the insulating film. Therefore, a light emitting device with a high degree of reliability can be realized.

[0140]

In this embodiment, only the structures of pixel portion and the driver circuit are  
15 shown. However, according to the manufacturing process of this embodiment, in addition to these, a signal dividing circuit, a D/A converter, an operational amplifier, and a logic circuit such as a correction circuit can be formed on the same insulator. Further, a memory and a microprocessor can also be formed thereon.

[0141]

20 A light emitting device according to this embodiment after the sealing (or encapsulating) process for protecting the light emitting elements has been performed will be described with reference to Fig. 13. Note that, like parts are indicated by like reference numerals in Fig. 12, if necessary.

[0142]

25 Fig. 13(A) is a top view showing a state where the light emitting element has been sealed, and Fig. 13(B) is a cross-sectional view of Fig. 13(A) taken along the line C—C'. Reference numeral 801 indicated by a dotted line denotes a source driver circuit, reference numeral 806 denotes a pixel portion, and reference numeral 807 denotes a gate driver circuit. Reference numeral 901 denotes a covering material, reference numeral 902 denotes a first  
30 sealing member, and reference numeral 903 denotes a second sealing member. A sealant 907 is provided inside an area enclosed by the first sealing member 902.

[0143]

Reference numeral 904 denotes wiring for transmitting a signal input to a source driver circuit 801 and a gate driver circuit 807. The wiring 904 receives a video signal and a  
35 clock signal from a FPC (flexible printed circuit) 905 that is an external input terminal.

Incidentally, though only the FPC is illustrated, a printed wiring board (PWB) may be attached to the FPC. The light emitting device in this specification refers not only to the main body of the light emitting device but also to the device to which the FPC or the PWB is attached.

[0144]

5           Next, a cross-sectional structure of the light emitting device will be described with reference to Fig. 13(B). The pixel portion 806 and the gate driver circuit 807 are formed on the substrate 700. The pixel portion 806 is composed of the current controlling TFT 604 and a plurality of pixels including the pixel electrode 710 electrically connected to the drain of the current controlling TFT 604. The gate driver circuit 807 is formed by using a CMOS circuit  
10       combining the n-channel TFT 601 and the p-channel TFT 602 (refer to Fig. 12).

[0145]

          The pixel electrode 710 functions as the anode for the light emitting elements. The banks 712 are formed on both sides of the pixel electrode 710. The light emitting layer 713  
— and the cathode 714 for the light emitting elements are formed over the pixel electrode 710.

15       [0146]

          The cathode 714 also functions as the wiring common to all the pixels, and is electrically connected to the FPC 905 via the connection wiring 904. All the elements contained in the pixel portion 806 and the gate driver circuit 807 are covered with the cathode 714 and the passivation film 567.

20       [0147]

          The covering material 901 is bonded together by the first sealing member 902. Spacers formed of a resin film may also be provided so as to ensure spacing between the covering material 901 and the light emitting element. Then, the area inside the first sealing member 902 is filled with a sealant 907. Preferably, an epoxy resin is used for the first sealing  
25       member 902 and the sealant 907. Further, preferably, the first sealing member 902 is formed of a material that inhibits permeation of moisture and oxygen as effectively as possible. Still further, a moisture absorbent or a oxidation inhibitor may be contained in the sealant 907.

[0148]

          The sealant 907 provided so as to cover the light emitting element also functions as an  
30       adhesive for bonding the covering material 901. In this embodiment, FRP (fiberglass-Reinforced Plastics), PVF (PolyVinyl Fluoride), Mylar, polyester, or acrylic can be employed for a material of a plastic substrate 901a constituting the covering material 901.

[0149]

          After the covering material 901 is bonded using the sealant 907, the second sealing  
35       member 903 is provided to cover the sides (exposed surfaces) of the sealant 907. As a material

for the second sealing members 903, the same material as that for the first sealing member 902 can be employed.

[0150]

Encapsulation of the light emitting element in the sealant 907 with the structure  
5 described above allows the light emitting element to be completely blocked from the outside. Entering of a substance such as moisture or oxygen from the outside, which promotes deterioration of the light emitting layer by oxidation, can be thereby prevented. Therefore, the light emitting device with high reliability can be obtained.

[0151]

10 Note that, this embodiment can be freely combined with any one of Embodiments 1 thorough 4 or Embodiment 7.

[0152]

[Embodiment 8]

15 In this embodiment, a light emitting device having a pixel structure different from that in Embodiment 7 will be described. Fig. 14 is used for explanation.

[0153]

Referring to Fig. 14, a TFT that has the same structure as the n-channel TFT 601 in Fig. 11 is employed as a current controlling TFT 4501. The gate electrode of the current  
20 controlling TFT 4501 is of course electrically connected to the drain wiring of a switching TFT 4402. The drain wiring of the current controlling TFT 4501 is electrically connected to a pixel electrode 4504.

[0154]

In this embodiment, the pixel electrode 4504 formed of a conductive film functions as the cathode for light emitting elements. Specifically, an alloy film of aluminum and lithium is  
25 employed for the pixel electrode 4504. However, a conductive film made from an element belonging to Group 1 or Group 2 of the periodic table, or a conductive film added with these elements may be employed.

[0155]

A light emitting layer 4505 is formed over the pixel electrode 4504. Though only  
30 one pixel is illustrated in Fig. 14, a light emitting layer that corresponds to G (green) is formed by the vapor deposition method or the application method (preferably spin coating) in this embodiment. Specifically, the light emitting layer 4505 comprises layered structure of a film of lithium fluoride having a thickness of 20nm as an electron injecting layer and a PPV (polyparaphenylenevinylene) film having a thickness of 70nm superimposed thereon as the light  
35 emitting layer.

[0156]

Next, an anode 4506 formed of a transparent conductive film is provided on the light emitting layer 4505. In this embodiment, a conductive film formed of a compound of indium oxide and tin oxide or a compound of indium oxide and zinc oxide is employed as the  
5 transparent conductive film.

[0157]

Upon formation of the anode 4506, a light emitting element 4507 is completed. The light emitting elements 4507 herein refer to diodes formed of the pixel electrode (cathode) 4504, the light emitting layer 4505, and the anode 4506.

10 [0158]

It is effective to provide a passivation film 4508 such that the light emitting elements 4507 are completely covered with the passivation film. The passivation film 4508 is formed of an insulating film including a carbon film, silicon nitride film, or silicon oxynitride film. The insulating film is used in a single layer of one of these films or a lamination of these films.

15 [0159]

Further, a sealant 4509 is provided over the passivation film 4508, and a covering material 4510 is bonded to the sealant 4509. The ultraviolet cured resin may be used for the sealant 4509, and it is effective to provide therein a moisture absorbent or a oxidation inhibitor. In this embodiment, the covering material 4510 in which a carbon film (preferably diamond-like carbon film) is formed on both sides of a glass substrate, a quartz substrate, or a plastic substrate (including the plastic film), is employed.  
20

[0160]

Note that this embodiment can be freely combined with any one of Embodiments 1 through 4 of Embodiment 9.

25 [0161]

[Embodiment 9]

In this embodiment, an active matrix substrate having a TFT structure different from that on the substrate manufactured according to Embodiments 4 and 7 will be described. Then, a liquid crystal display device manufactured according to the present invention will be  
30 described.

[0162]

On an active matrix substrate shown in Fig. 15(A), a driver circuit 506 having an n-channel TFT 503 and a p-channel TFT 502, and a pixel portion 507 having a pixel TFT 504 and a storage capacitor 505 are formed.

[0163]

These TFTs are manufactured by first forming gate wirings 512 to 517 over a substrate 510, forming an insulating film 511 over the gate wirings, and then providing the channel forming region, source region, drain region, LDD region, or the like over the semiconductor layer on the insulating film. The semiconductor layer is formed according to the present invention, as in Embodiments 1 through 5.

[0164]

The gate wirings 512 to 517 are formed with a thickness of 200 to 400nm (preferably a thickness of 250nm), and the ends of the gate wirings are tapered so as to improve the step coverage of the films to be formed thereon. The angle of the tapered portions is from 5 to 30 degrees (preferably from 15 to 25 degrees). The tapered portions are formed by dry etching. The angle of the tapered portions is controlled by the etching gas and a bias voltage applied to the substrate.

[0165]

Impurity regions are formed by first through third doping processes. First, the first doping process is carried out to form an LDD (Lightly Doped Drain) region of the n-channel TFT. The doping may be carried out by ion doping or ion implantation. Phosphorus (P) is doped as an impurity element (donor) for imparting the n-type conductivity, and first impurity regions 219 and 222 are formed by means of a mask. Then, another mask for covering the LDD region of the n-channel TFT is formed, and the second doping process is carried out to form the source and drain regions of the n-channel TFT.

[0166]

Then, the source and drain regions of the p-channel TFT are formed by the third doping process. The doping may be carried out by adding an impurity element (acceptor) for imparting the p-type conductivity by ion doping or ion implantation. Since a mask is formed on the semiconductor layer which forms the n-channel TFTs, the impurity element for imparting the p-type conductivity is not added. In this embodiment, the LDD region is not formed in the p-channel TFT. However, the LDD region may of course be formed.

[0167]

In this way, the LDD region 530 and a source or drain region 531 are formed outside a channel forming region 529 in the n-channel TFT 503. The p-channel TFT 502 has the similar structure, and is formed of a channel forming region 527 and a source or drain region 528. In this embodiment, the TFTs take on the single-gate structure. However, they may also take on the double-gate structure or the triple-gate structure.

[0168]

In the pixel portion 507, the pixel TFT 504 formed of an n-channel TFT is formed in the multi-gate structure in order to reduce the off-state current. The LDD region 533 and a source or drain region 534 are provided outside a channel forming region 532.

[0169]

5 The interlayer insulating films formed of a first interlayer insulating film 540 and a second interlayer insulating film 541. The first insulating film 540 is formed of an inorganic material such as silicon oxide, silicon nitride, or silicon oxynitride, and has a thickness of 50 to 500nm. The second interlayer insulating film 541 is formed of an organic insulating material such as polyimide, acrylic, polyimideamide, and BCB (benzocyclobutene). Forming the second  
10 interlayer insulating film of the organic insulating material in this manner allows the surface of the film to be planarized well. Further, generally, the dielectric constant of organic resin materials is low, so that the parasitic capacitance can be reduced. However, organic materials have hygroscopicity, so that they are not suitable to be used as the protective film. Accordingly, it is preferable that the second interlayer insulating film 541 is formed in combination with the  
15 first interlayer insulating film 540.

[0170]

Thereafter, a resist mask having a predetermined pattern is formed, and then contact holes that extend to the source region or the drain region formed in the respective semiconductor layers are formed. Formation of the contact holes is carried out by dry etching.  
20 In this case, a mixture of  $\text{CF}_4$ ,  $\text{O}_2$ , and He is used as the etching gas to first etch the second interlayer insulating film 541 formed of the organic resin material. Then,  $\text{CF}_4$  and  $\text{O}_2$  are used as the etching gas to etch the first interlayer insulating film 540.

[0171]

Then, a conductive metal film is formed by sputtering or vacuum deposition to form a  
25 resist mask pattern. Thereafter, wirings 543 to 549 are formed by etching. In this way an active matrix substrate can be formed.

[0172]

A process of manufacturing an active matrix liquid crystal display using the active matrix substrate in Fig. 15(A) will be described. Fig. 15(B) shows the state where the active  
30 matrix substrate and a counter substrate 554 are bonded together by means of a sealing member 558. First, columnar spacers 551 and 552 are formed on the active matrix substrate in Fig. 15(A). The spacers 551 of the pixel portion are provided so as to overlap with contact portions on the pixel electrode. Though depending on what is used in a liquid crystal, the height of the spacer is arranged to be 3 to 10 $\mu\text{m}$ . In the contact portions, a recess corresponding to the  
35 contact holes are formed. Therefore, by forming the spacers at positions to coincide with this

portion, disturbance of the orientation of liquid crystals can be prevented. Thereafter, an orientation 553 is formed and a rubbing process is carried out. A transparent conductive film 555 and an orientation film 556 are formed on the counter substrate 554. Thereafter, the counter substrate and the active matrix substrate are bonded together and the liquid crystal is injected.

[0173]

The active matrix liquid crystal display devices manufactured as described above can be used as displays for various electronic devices.

[0174]

This embodiment can be freely combined with any one of Embodiments 1 thorough 4 or Embodiment 7.

[0175]

[Embodiment 10]

In this embodiment, a light emitting device manufactured with the active matrix substrate explained in Embodiment 9 will be described.

[0176]]

Referring to Fig. 16, a TFT that has the same structure as the n-channel TFT 503 in Fig. 15 is employed as the current controlling TFT 4501. The gate electrode of the current controlling TFT 4501 is, of course, electrically connected to the drain wiring of the switching TFT 4402. The drain wiring of the current controlling TFT 4501 is electrically connected to the pixel electrode 4504.

[0177]

In this embodiment, the pixel electrode 4504 formed of a conductive film functions as the cathode for light emitting elements. Specifically, an alloy film of aluminum and lithium is employed for the pixel electrode 4504. Here, a conductive film made from an element belonging to Group 1 or Group 2 of the periodic table, or a conductive film doped with these elements may be employed.

[0178]

The light emitting layer 4505 is formed over the pixel electrode 4504. Note that, though only one pixel is illustrated in Fig. 16, a light emitting layer that corresponds to G (green) is formed by the vapor deposition method or the application method (preferably spin coating) in this embodiment. Specifically, the light emitting layer 4505 comprises layered lamination of the film of lithium fluoride (LiF) having a thickness of 20nm as the electron injecting layer and the PPV (polyparaphenylenevinylene) film having a thickness of 70nm.

[0179]

Next, the anode 4506 formed of a transparent conductive film is provided on the light emitting layer 4505. In this embodiment, a conductive film formed of a compound of indium oxide and tin oxide or a compound of indium oxide and zinc oxide is employed as the  
5 transparent conductive film.

[0180]

Upon formation of the anode 4506, a light emitting element 4507 is completed. The light emitting element 4507 herein refers to diodes that comprise the pixel electrode (cathode) 4504, the light emitting layer 4505, and anode the 4506.

10 [0181]

It is effective to provide the passivation film 4508 such that the light emitting element 4507 is completely covered with the film. The passivation film 4508 is formed of an insulating film including a carbon film, silicon nitride film, or silicon oxynitride film. A single layer of  
--- one of these films or a lamination of these films is used. ---

15 [0182]

Further, the sealant 4509 is provided over the passivation film 4508, and the covering material 4510 is bonded together with the sealant 4509. An ultraviolet cured resin may be used for the sealant 4509, and it is effective to provide therein a substance that has the effect of absorbing moisture or preventing oxidation. In this embodiment, the covering material 4510 in  
20 which a carbon films (preferably diamond-like carbon film) is formed on both sides of the glass substrate, quartz substrate, or plastic substrate (including the plastic film) is employed.

[0183]

Note that, this embodiment can be freely combined with any one of Embodiments 1 through 4 or Embodiment 9.

25 [0184]

[Embodiment 11]

The CMOS circuit and the pixel portion formed by applying the present invention can be applied to various electro-optic devices (active matrix liquid crystal display device, active matrix EC display device or active matrix light emitting device). Specifically, the present  
30 invention can be embodied in electronic equipment of any type in which such an electro-optic device is incorporated in the display portion.

[0185]

As such electronic equipments, a video camera, a digital camera, a projector, a head-mounted display (goggle type display), a car navigation system, a car stereo, a personal  
35 computer, and a mobile information terminal (such as a mobile computer, a mobile telephone or

an electronic book) are given as examples. Figs. 17, 18, and 19 show the examples.

[0186]

Fig. 17(A) shows a personal computer, which includes a body 3001, an image input portion 3002, a display portion 3003, a keyboard 3004 and the like. The present invention can be applied to the display portion 3003.

[0187]

Fig. 17(B) shows a video camera, which includes a body 3101, a display portion 3102, an audio input portion 3103, operating switches 3104, a battery 3105, an image receptor 3106 and the like. The present invention can be applied to the display portion 3102.

10 [0188]

Fig. 17(C) shows a mobile computer, which includes a body 3201, a camera portion 3202, an image receptor 3203, an operating switch 3204, a display portion 3205 and the like. The present invention can be applied to the display portion 3205.

[0189]

15 Fig. 17(D) shows a goggle type display, which includes a body 3301, a display portion 3302, arm portions 3303 and the like. The present invention can be applied to the display portion 3302.

[0190]

20 Fig. 17(E) shows a player using a recording medium on which a program is recorded (hereinafter referred to as the recording medium), and the player includes a body 3401, a display portion 3402, speaker portions 3403, a recording medium 3404, operating switches 3405 and the like. This player uses a DVD (Digital Versatile Disc), a CD and the like as the recording medium, and enables a user to enjoy music, movies, games and the Internet. The present invention can be applied to the display portion 3402.

25 [0191]

Fig. 17(F) shows a digital camera, which includes a body 3501, a display portion 3502, an eyepiece portion 3503, operating switches 3504, an image receptor (not shown) and the like. The present invention can be applied to the display portion 3502.

[0192]

30 Fig. 18(A) shows a front projector, which includes a projection device 3601, a screen 3602 and the like. The present invention can be applied to a liquid crystal display device 3808 which forms a part of the projection device 3601 as well as other driver circuits.

[0193]

Fig. 18(B) shows a rear projector, which includes a body 3701, a projection device

3702, a mirror 3703, a screen 3704 and the like. The present invention can be applied to the liquid crystal display device 3808 which forms a part of the projection device 3702 as well as other driver circuits.

[0194]

5 Fig. 18(C) shows one example of the structure of each of the projection devices 3601 and 3702 which are respectively shown in Figs. 18(A) and 18(B). Each of the projection devices 3601 and 3702 is formed of an optical light source 3801, mirrors 3802 and 3804 to 3806, a dichroic mirror 3803, a prism 3807, a liquid crystal display device 3808, a retardation film 3809 and an optical projection system 3810. The optical projection system 3810 is formed of  
10 an optical system including a projection lens. This embodiment is an example of a three-panel system, but it is not limited to this example and a single-panel system may also be used. In addition, the operator may appropriately dispose an optical system such as an optical lens, a polarization film, a film for adjusting the phase difference, or an IR film in the path indicated by arrows in Fig. 18(C).

15 [0195]

Fig. 18(D) is a view showing one example of the structure of the optical light source 3801 shown in Fig. 18C. In this embodiment, the optical light source 3801 is formed of a reflector 2811, a light source 3812, lens arrays 3813 and 3814, a polarization conversion element 2815 and a condenser lens 3816. Incidentally, the optical light source shown in Fig.  
20 18(D) is one example, and the present invention is not particularly limited to the shown construction. For example, the operator may appropriately dispose an optical system such as an optical lens, a polarizing film, a film for adjusting the phase difference or an IR film.

[0196]

However, the projector shown in Fig. 18 is of the type using a transparent type of  
25 electro-optic device, an example in which the invention is applied to a reflection type of electro-optic device and a light-emitting device is not illustrated.

[0197]

Fig. 19(A) shows a mobile telephone, which includes a body 3901, a audio output portion 3902, a audio input portion 3903, a display portion 3904, operating switches 3905, an  
30 antenna 3906 and the like. The present invention can be applied to the display portion 3904.

[0198]

Fig. 19(B) shows a mobile book (an electronic book), which includes a body 4001, display portions 4002 and 4003, a storage medium 4004, operating switches 4005, an antenna 4006 and the like. The invention can be applied to the display portions 4002 and 4003.

35 [0199]

Fig. 19(C) shows a display, which includes a body 4101, a stand 4102, a display portion 4103 and the like. The present invention can be applied to the display portion 4103. The present invention is particularly advantageous to a large-screen display, and is advantageous to a display having a diagonal of 10 inches or more (particularly, 30 inches or more).

[0200]

As described above, the present invention is capable of extremely wide application, and the invention can be applied to any category of electronic devices. Further, electronic devices of the present embodiment can be realized by using a structure of any combination according to Embodiments 1 to 10.

[0201]

[Effect of the Invention]

By applying the present invention, TFTs having high mobility can be formed. In addition, semiconductor devices typified by a high-definition active matrix liquid crystal display device and a light emitting device can be manufactured.

[Brief Description of the Drawings]

- [Fig. 1] Views showing examples of a concept of the present invention;
- [Fig. 2] Views showing examples of a concept of the present invention;
- [Fig. 3] Views showing examples of a concept of the present invention;
- 20 [Fig. 4] Cross-sectional views showing the process of manufacturing pixel TFTs and driver circuit TFTs;
- [Fig. 5] Cross-sectional views showing the process of manufacturing pixel TFTs and driver circuit TFTs;
- [Fig. 6] Cross-sectional views showing the process of manufacturing pixel TFTs and driver circuit TFTs;
- 25 [Fig. 7] Cross-sectional views showing the process of manufacturing pixel TFTs and driver circuit TFTs;
- [Fig. 8] A top view showing pixels in a pixel portion;
- [Fig. 9] A cross-sectional view showing a process of manufacturing an active matrix liquid crystal display device;
- 30 [Fig. 10] A cross-sectional view showing a process of manufacturing an active matrix liquid crystal display device;
- [Fig. 11] A cross-sectional view showing a process of manufacturing pixel TFTs and driver circuit TFTs;

- [Fig. 12] A cross-sectional view showing the structure of a driver circuit and a pixel portion in a light emitting device;
- [Fig. 13] (A) A top view of a light emitting device;
- (B) A cross-sectional view showing the structure of a driver circuit and a pixel portion in the light emitting device;
- 5 [Fig. 14] A cross-sectional view showing the structure of a pixel portion in a light emitting device;
- ~~[Fig. 15] (A) A cross-sectional view showing a process of manufacturing an active matrix substrate;~~
- 10 (B) A cross-sectional view showing a process of manufacturing an active matrix liquid crystal display device;
- [Fig. 16] A cross-sectional view showing the structure of a pixel portion in a light emitting device;
- [Fig. 17] A diagram showing examples of semiconductor devices;
- 15 [Fig. 18] A diagram showing examples of semiconductor devices;
- [Fig. 19] A diagram showing examples of semiconductor devices.

[Name of Document]      Abstract

[Summary]

[Problem]

5      When a laser beam is radiated onto a semiconductor film, an abrupt temperature gradient is produced between a substrate and the semiconductor film. For this reason, the semiconductor film contracts, so that a strain in the film occurs. Therefore, the quality of thus obtained crystalline semiconductor film may be deteriorated.

[Solving Means]

10      The present invention is characterized in that, after laser beam crystallization of the semiconductor film, a heat treatment is carried out so as to lessen the strain in the film. Since the substrate contracts by the heat treatment, the strain formed in the semiconductor film is lessened, so that the physical properties of the semiconductor film can be improved.

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